REMARKS

I. Introduction

These amendments and remarks are being filed in response to the Office Action dated January 7, 2009. Claims 1-13, 15, 18 and 19 are pending. Claims 14, 16 and 17 were previously cancelled. Claims 5, 6, 9-11 18 and 19 were withdrawn by the Examiner following a Restriction Requirement. Applicants acknowledge, with appreciation, the Examiner's allowance of Claim 4.

Claim 12 has been amended to incorporate elements of allowed claim 4. Applicants thank Examiner Kretelia Graham for participating in the interview with Applicants and Applicants representatives on May 19, 2009. During the interview the Examiner helpfully explained the basis of her rejections, facilitating Applicants response. The amendment of claim 12, was discussed and agreed that the amendment would overcome the rejections over the cited prior art. Furthermore, Applicants discussed the allowability of claims 1-4, 7-9, 13 and 15.

The foregoing amendments and for the following reasons, Applicants respectfully submit that the claims are allowable and request that the application be passed to issue.

No new matter has been added.

II. Claim Rejections Under 35 U.S.C. § 102(b) or, in the alternative § 103(a)

Claims 1 and 3 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Oda U.S. Patent No. 5,644,387. Applicants respectfully disagree.

Claim 1 recites, in pertinent part, "A memory matrix device for storing temporally sequential information in a manner that retains the sequence of information without dependence

on multiple memory addresses, **and is not a serial sequential access memory, a random access memory or a dynamic random access memory**." [Emphasis added].

As known to a person having ordinary skill in the art, serial sequential access memory means that a group of elements is accessed in a predetermined, ordered sequence. Moreover, as it pertains to data structures, sequential access means that the values it contains can only be visited once in one particular order.

Oda describes such a serial sequential access memory (first in first out, "FIFO"), in which the even latches "i.e., the LAST-6 latch, LAST-4 latch, and then the LAST-2 latch are updated, in that order, information is transferred serially from one register to another. On the next enable, the "odd" latches i.e., the LAST-5 latch, LAST-3 enable, the "odd" latches, i.e., the LAST-5 latch, LAST-3 latch, and then the LAST-1 latch are updated again in that order," (see col. 6, line 63 – col. 7, line 1). [Emphasis added]. Updating of the latches occurs serially by transfer of information from one register to the next through Q outputs to D inputs, (see Oda col. 4 lines 17-23 and FIGS. 3 and 4). As such, Oda is directed to a serial sequential (FIFO) access memory.

In contrast, in the subject matter as recited in claims 1, each array becomes enabled and then unenabled in temporal sequence, thereby directing the next temporal bit of information to the next memory storage unit in said sequentially-connected array.

Therefore, it is clear that Oda does not teach or suggest all of the elements of claim 1. Accordingly, it is respectfully submitted that claim 1 is allowable. Furthermore, claim 3 depends from claim 1 and therefore is also allowable.

III. Claim Rejections under 35 U.S.C. § 102(b)

Claims 2, 7, 8 , 13 and 15 were rejected under 35 U.S.C. § 102(b). Applicants respectfully disagree. As discussed above, regarding the rejection of claims 1 and 3 as allegedly being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Oda, Applicants respectfully submit that Oda fails to disclose all of the elements of claim 1. This is because at a minimum, Oda fails to disclose A memory matrix device for storing temporally sequential information in a manner that retains the sequence of information without dependence on multiple memory addresses, **and is not a serial sequential access memory, a random access memory or a dynamic random access memory**." [Emphasis added].

Similarly, claim 7 recites, in pertinent part, "A memory matrix device for storing temporally sequential information in a manner that retains the sequence of information without dependence on multiple memory addresses, **and is not a serial sequential access memory, a random access memory or a dynamic random access memory**." [Emphasis added]. Updating of the latches occurs serially through transfer of information from one register to the next through Q outputs to D inputs, (see Oda col. 4 lines 17-23 and FIGS. 3 and 4). As such, Oda is directed to a FIFO sequential access memory.

Oda describes such a serial sequential access memory in which the even latches "i.e., the LAST-6 latch, LAST-4 latch, and then the LAST-2 latch are updated, in that order. On the next enable, the "odd" latches i.e., the LAST-5 latch, LAST-3 enable, the "odd" latches, i.e., the LAST-5 latch, LAST-3 latch, and then the LAST-1 latch are updated again in that order," (see col. 6, line 63 – col. 7, line 1). [Emphasis added].

In contrast, in the subject matter as recited in independent claims 1 and 7, each array becomes enabled and then unenabled in temporal sequence, thereby directing the next temporal bit of information to the next memory storage unit in said sequentially-connected array, and

Furthermore, independent claim 13 recites, in pertinent part "that the fixed memory storage units of said array are written to and latched in an invariant order; and whenever a signal generator activates reading at the first fixed memory storage unit of the array, reading of the entire array of fixed memory storage units occurs in the same invariant order."

This method reads the full sequence of the stored data in time and space.

In contrast, Oda does not provide a method for later retrieving the original data in its original sequence. Instead, Oda discloses an instrument which stores secondary information derived from a calculation (e.g., the time-delay between the first and last data point), and must be reset prior to the initiation of a second reading. As such, Oda clearly does not teach a method for replaying the stored information for reanalysis, or to replay the information on repeated occasions.

Therefore, it is clear that Oda does not teach or suggest all of the elements of claims 1, 7 and 13. Accordingly, claim 1, 7 and 13 are allowable. Furthermore, claim 2, 3, 8, 9 and 15 depend from and further define the subject matter of claims 1, 7 and 13 respectively, and therefore are also allowable.

IV. Claim Rejections Under 35 U.S.C. § 102(e)

Claim 12 was rejected under 35 U.S.C. § 102(e) as allegedly being unpatentable over Pomet U.S. Patent No. 5,963,505. Applicants respectfully disagree. However, claim 12 has been amended and now recites, in pertinent part,

> A memory matrix device for retrieving temporally sequential information, without processing multiple memory addresses, comprising:
>
> means for activating a pulse generator or other signal generator to read previously-stored information in sequentially-connected arrays of fixed memory storage units in the sequential order in which said fixed memory storage units are connected . . .
>
> **wherein said pulse generator or other signal generator has a frequency which is synchronized to the frequency of retrieved information, and**
>
> **wherein, said pulse generator or other signal generator simultaneously reads all fixed memory storage units of the same sequential order in all parallel sequentially-connected arrays, through connections that are functionally perpendicular to those of the sequentially-connected arrays.**

[Emphasis added].

In contrast to claim 12, Pomet does not disclose a pulse generator or other signal generator having a frequency which is synchronized to the frequency of retrieved information, and wherein, said pulse generator or other signal generator simultaneously latches all fixed memory storage units of the same sequential order in all parallel sequentially-connected arrays, through connections that are functionally perpendicular to those of the sequentially-connected arrays.

As such, Pomet fails to disclose all of the elements of amended claim 12. Accordingly, claim 12 is allowable.

V. Conclusion

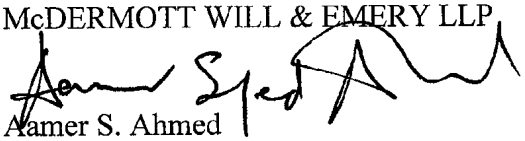
In view of the above amendments and remarks, Applicants respectfully submit that this application should be allowed and the case passed to issue. Moreover, withdrawn claims 5-6 depend from allowable generic claim 1; claims 10 and 11 depend from allowable generic claims 7, and claims 18 and 19 depend from allowable generic claim 13, and therefore should be rejoined pursuant to M.P.E.P. §809 and allowed.

If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Aamer S. Ahmed
Registration No. 58,958

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 ASA:MWE
Facsimile: 202.756.8087
Date: June 4, 2009

Please recognize our Customer No. 20277 as our correspondence address.